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Implementation of Smart Sensor with Frequency To Digital Convertor For Flow Measurement Using FPGA

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ABSTRACT

The realization of integrated frequency-based smart sensor for flow measurement requires a precise frequency to digital converter. A VHDL-based implementation of such converter for a royalty-free solution with 1 p pm resolution is reported. This work is part of a correlator under development to measure total flow of multiphase fluids. This intellectual property block can also be used with other frequency encoded transducers. The converter has been prototyped with a Xilinx TM XC3S500E Spartan-3E FPGA, and has been tested up to 10MHz.

1. Introduction

Cross-correlation can be used to measure flow in a multiphase fluid One has to be careful with the detected signal, as it is mixed with noise. Wavelet transform techniques may be used to improve the correlator performance in such conditions [1, 2, 3, 4, 5].For the purpose of this work, piezoelectric and capacitance transducers are used as part of an oscillator circuit, such as, Colpitts or Pierce. The oscillator is then connected to a frequency to digital converter, see Fig. 1. Frequency encoded information has several advantages as compared to other analog sensor output, such as: high noise immunity, output signal power, wide dynamic range, high accuracy of frequency standards. The generated signal is detected, processed and transmitted by a smart sensor. The controller and correlator core with real time features is also under development, including special digital signal processing techniques. The communication interface is a Controller Area Network - CAN module, which has been reported previously [6, 7, 8].

Fig: 1. Block diagram of proposed flow meter. In this paper, a precise frequency to digital converter VHDL core is reported. Several topologies of conversion are found in the literature, and some of them have become commercial products, one such example which can be implemented in FPGA (Field Programmable Gate Array) is from Auto TEC [9]. Other examples are the UFDC-1 [7, 10, 11] and UFDC-2 [12, 13]. A variant is the time to frequency converter, as implemented in references [14, 15]. The objective is to design a converter capable of working in a wide frequency range. This VHDL block will be combined with analog and RF blocks to build an Application Specific Integrated Circuit - ASIC. At this stage, the FPGA is used to validate and mature the design. Thus, the need to develop this IP core for a royalty-free solution.

This paper is divided into 5 sections. This introduction is the 1st; next, a brief review about flow measurement is presented. In Section3rd, the methods of conversion are described; explanations are presented in terms of the conversion time and accuracy. The 4th section presents the results and analysis. Final one is conclusions. Flow rate is adjusted with a 3-phase inverter connected to a Programmable Logic Controller - PLC.

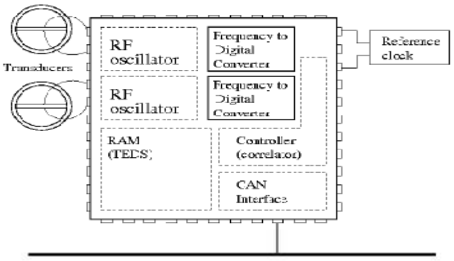

Fig. 1. Block diagram of proposed flowmeter.

2. Flow Measurement

One of the most utilized techniques for flow measurement is based on the differential pressure. This includes: orifice plate, nozzle and Venturi nozzle. The basic equation for volumetric flow rate is displayed in Equation 1.

$$\dot{Q} = C_d Y A \sqrt{\frac{2(1/\rho)\Delta p}{1-\beta^4}} \qquad (1)$$

where Cd is the discharge coefficient, it is related to friction, varying with the Reynolds number; Y is related to he fluid compressibility, Y = 1 for incompressible fluids; Δp is the measured differential pressure; $\beta = d/D$ is the diameter ratio, A is the cross-sectional area of the pipe, and ρ is the fluid density. Some typical values are $0.4 < \beta < 0.75,\ 50mm < D < 250mm,$ And Reynolds number over 105. To get the mass flow-rate, ˙M , from Equation 1, it is enough to multiply ˙Q by the fluid density. For multiphase flow with no phase slipping, Equation 1 is adapted by replacing the fluid density with a combined density. One such possibility is the linear combination of the individual phase densities. Phase slipping occurs when different phases in the flow have different velocities. In this work, it assumed that all phases have the same velocity. Circuit [6].

3. Methods for Frequency to Digital Conversion

Several conversion methods are described in the literature [7, 9, 10, 11, 16, 17]. An FPGA-based implementation is supplied by Auto TEC, with 16-bit and 12-bit counters and a 1MHz clock frequency as reference. The conversion range is from 35Hz to 24 kHz, with absolute error ±5Hz [9]. Disadvantages of these topologies are low accuracy and narrow input frequency range. The Universal Frequency to Digital Converters, UFDC-1 and UFDC-2, are also commercial converters, sold as an of the- shelf chip.. This method consists in the separation but simultaneous counting of the periods of the frequency to be measured and that of a reference frequency until a program specified number of pulses is obtained. They can be used for the measurement of frequency, period, their ratios, duty cycle and phase-shift [7, 10, 11]. UFDC-1 features a frequency range from 0.05Hz to 7.5MHz (120MHz with pre scaling), programmable accuracy from 1% to 0.001%, and the conversion time can be determined from Equation 2.[19].

$$t_{x_{min}} = \frac{1}{f_0 \delta_q} \qquad (2a)$$

$$t_{x_{max}} = \frac{N_\delta + f_0/f_x}{f_0} \qquad (2b)$$

Where f0 and fx are the reference and the input signal frequency, respectively, δ_q the quantization error and $N_\delta = 1/\delta_q$. Its conversion times limits are 0.0002 − 0.2 s. UFDC-2 has an extended frequency range: 0.05Hz to9MHz (144MHz with pre scaling), increased accuracy: 1% to 0.0005%, and shorter conversion time: 0.00016 − 0.32 s. It is based in the novel modified method of the dependent count [13]. Many performance comparisons are presented in reference [12]. The method selected for our application can achieve a better accuracy, 1 ppm (0.0001%), and convert frequencies up to 10MHz (without pre scaling), as compared to the methods found in the literature. This method consists in counting how many cycles of the input signal, Nis, occurs in a given number of clock cycles, Nck. The clock frequency must be stable and accurately measured. An illustration of the measurement method is shown in Fig. 2 this technique is widely used for frequency to digital conversion [7, 9, 10, 13, 15, 16, 18].

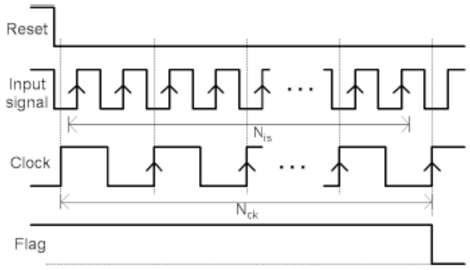

Fig: 2. Waveforms to illustrate the measurement method

The block diagram of the implemented converter is shown in Fig. 4. To achieve a precise measurement, two counters are used; one counts a pre-defined number of cycles of a stable and well known clock (CLOCK COUNTER), during this counting period, the other counts the cycles of the input signal (IN SIGNAL COUNTER). When the clock counter reaches its pre-defined final count, the output of the IN SIGNAL COUNTER is read. The maximum converted frequency is just below the frequency which causes a counter overflow.

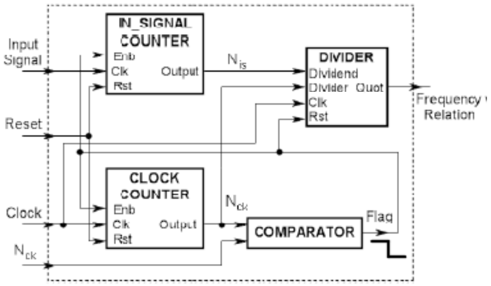

Fig: 3. Block diagram of the frequency to digital converter.

Next, both counter outputs are fed to a divider to calculate the ratio Nis/Nck. Finally, the frequency is obtained by a multiplication with the clock frequency, as shown in Equation 3. The input signal is not synchronized with the clock signal: they are, in fact, two totally unrelated signals. Due to this, a maximum error of ±1 count should be considered in the response of the converter.[19].

$$f_{is} = f_{ck}\left(\frac{N_{is}}{N_{ck}} \pm \frac{1}{N_{ck}}\right) \qquad (3)$$

This multiplication step can be avoided by renormalization of the unit of frequency. For this application a clock frequency of 1MHz is used, therefore the digital output is understood to be in MHz. The precision of the division step determines the overall precision of the converter. To reduce counting error in the input signal counter synchronization is established: the input signal counter starts only after the first clock signal rising transition with RESET in low level. The accuracy, $^{\delta}$ of conversion is given by Equation 4. This equation indicates the measured uncertainty, in units of frequency, for a given input signal frequency.

$$\delta = \frac{f_{ck}}{N_{ck}} \qquad (4)$$

The input signal counter must have at least the same number of bits as the clock counter. Increasing the number of bits allows for the measurement of higher frequencies. A RESET signal is used to put the system in initial condition: if it is set to high, all the outputs are reset to zero. An automatic RESET mechanism has been introduced allowing the converter to perform continuous measurements. With Equation 5, one can estimate the conversion time, t. Conversion time increases as a higher accuracy is required, as shown in Fig.4.

$$t = \frac{N_{ck}}{f_{ck}} \qquad (5)$$

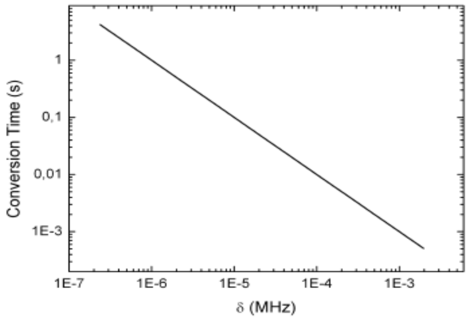

Fig: 4. the dependence between conversion time (t) and accuracy

The division operation is performed through shifts, which can be used to divide any two numbers, as long as the divider is a power of two. An implementation example with two decimal digits is shown in Fig 5. To ease the result presentation, the divider has been implemented on base 10 format. The divider basic blocks (DIV IDER) is organized in cascade to allow the division of the rest. Therefore, the input divider Nck must be of the form 2n, where n is a integer. A stage to multiply by ten has been implemented with shifts and addition (MULT 10). The FINISH signal (present in each divider basic block) generates a pulse with the width 23 of the clock period when the calculation ends. This signal is required for the initialization of a next divider basic block.

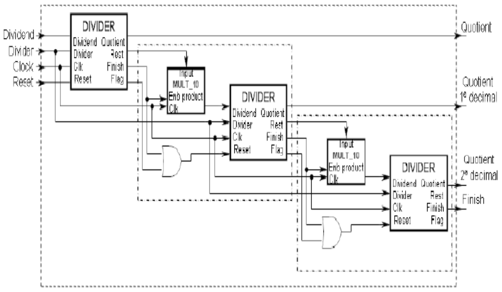

Fig: 5. Block diagram for the divider with two decimal digits

4. Results and Analysis

4.1. Synthesis The design has been implemented, simulated and synthesized using Xilinx design tools. The synthesis is carried out with a Spartan-3E (XC3S500E Spartan-3E FPGA) starter kit board [20]. Each block was validated separately, and later combined to form the converter. The FPGA utilization is about 50% for a 30-bit clock counter and a 30-bit input signal counter. The summary also indicates that the maximum frequency that can be converted is about 16MHz [19].

The stable RF generator signal is used as clock after conditioning. The measurement results are updated at the end of each conversion cycle and presented on the starter kit board LCD display. The LCD display code is based on an example from reference [21]. The frequency is also measured with an HP53181A precision frequency meter for comparison. A converter with 30-bit wide counter, a clock frequency of 1MHz, and Nck =220 has been synthesized. The conversion process starts as the RESET signal is set to low level. The measurements display a 1 p pm error, as compared to the frequency meter. A plot of the relative error between frequency meter and converter is presented in Fig. 6. The initial points of the plot have a higher scattering, as the measurement data from the frequency meter presented more decimal digits than the converter data. Therefore the relative error increased. The converter works with a fixed amount of decimal digits unlike the frequency meter that adjusts automatically. However for frequencies above 500 kHz the relative error is less than 1 p pm.

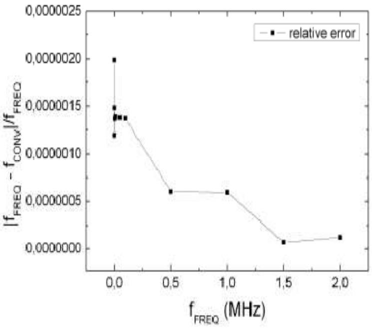

Fig: 6. Relative error for measures made from 100Hz to 2MHz compared to the frequency meter (fFREQ).

With Equation 5, one can estimate the conversion time. For this implementation Nck/fck = 1 s, the processing time of division stage is much smaller than this one. The measurements are updated in the display every 1 s, ignoring the processing time to generate the LCD displays which is a few milliseconds. The converter response to a sudden change of the input signal frequency will be stabilized soon after one reading of the converter. Next, a Pierce-oscillator circuit was built. Different crystals were positioned in the XTAL component (see Fig. 7). The Vout signal was applied to an inverter, to convert the sinusoidal wave into a square wave. The output was applied to the frequency meter, as shown in Fig. 7. In this scheme, the clock signal is obtained from the 50MHz signal present in the development kit. This clock signal is divided down to 1MHz. The results of these two readings were similar until a particular decimal digit, from this decimal digit a fluctuation was observed in both devices, as can be seen in Table 1. The fluctuation is due to the instability presented in the oscillator circuit.

5. Conclusion

A precision frequency to digital converter has been synthesized in VHDL with Xilinx TM XC3S500E Spartan-3E FPGA. The proposed converter has been designed to work in a wide frequency range (100Hz to 10MHz), both above and below the reference frequency. A 1 ppm (0.0001%) precision has been achieved. To the author’s knowledge, the only converter close to this implementation is the UFDC-2 (0.0005%).

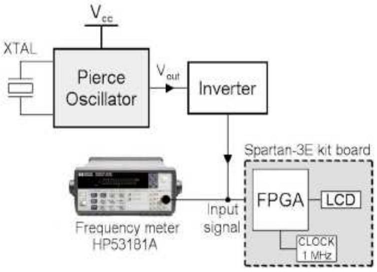

Fig: 7. Experimental apparatus for measuring crystals frequency.

Table: 1. Conformity between the converter and HP53181A frequency meter.

Crystal	Coincidence digits
X-cut (10 MH$_Z$)	10.0109 MH$_Z$
Y-cut (10 MH$_Z$)	9.924 MH$_Z$
Commercial (10 MH$_Z$)	9.998 MH$_Z$
Commercial (4 MH$_Z$)	3.9992 MH$_Z$

Frequencies as high as 10MHz can be converted with no pre-scaling, while UFDC-1 achieves 7.5MHz and UFDC- 2 achieves 9MHz. Using a stable, and well characterized reference clock, it can achieve a precision of 1 ppm. Simulations indicate the frequency above 100MHz can be converted. For this implementation the conversion time is 1 s. It is possible to reduce the conversion time, sacrificing the precision. The converter has been designed combining the behavioral and structural styles. Every block has been validated separately before integration. This combination of hierarchical design and well-define interfaces in each block gives a great deal of flexibility to the designer, and reduces the possibility of mistakes. This development is part of a smart flow meter under development. The precision is higher than the oscillator circuit. To get full benefit, a carefully designed oscillator circuit is required and it is under development. Further development should improve precision and conversion speed, as the possibility to measure signals with Pulse Width Modulation (PWM).

References

[1] M. S. Beck, “Correlation in instruments: cross correlation flowmeters,” J. Phys. E: Sci. Instrum., vol. 14, pp. 7–19, 1981.

[2] L. A. Xu, R. G. Green, A. Plaskowski, and M. S. Beck, “The pulsed ultrasonic cross-correlation flowmeter for two-phase flow measurement,” J. Phys. E: Sci. Instrum., vol. 21, 1988.

[3] W. Q. Yang and M. S. Beck, “An intelligent cross correlator for pipeline flow velocity measurement,” Flow. Meas. Instrum., vol. 8, no. 2, 1997.

[4] L. H. Sibul and L. G. Weiss, “A wideband wavelet based estimator correlator and its properties,” Multidimensional Systems and Signal Processing, vol. 13, 2002.

[5] J. M. I. Muoz, D. Dellvale, M. O. Sonnaillon, and F. J. Bonetto, “Real-time particle image velocimetry based on fpga technology,” in Proc. of the 5th Southern Conference on Programmable Logic, SPL 2009, 2009, pp. 147–152.

[6] E. J. P. Santos, P. L. Guzzo, and A. H. Shinohara, “Development of quartz-based smart pressure sensor for oil wells,” in Proc. XIX Eurosensors, Barcelona, 2005.

[7] S. Y. Yurish and N. Kirianaki and R. Pall`as-Areny, “Universal frequency-to-digital converter for quasi-digital and smart sensors: specifications and applications,” Sensor Review, vol. 25, no. 2, pp. 92–99, 2005.

[8] J. E. O. Reges and E. J. P. Santos, “A VHDL CAN module for smart sensors,” in Proc. IV Southern Conference on Programmable Logic, 2008.

[9] http://www.autotecsystems.com.[10] S. Y. Yurish, “Digital sensors design based on universal frequency sensors interfacing ic,” Sensors and Actuators A: Physical, vol. 132, pp. 265–270, 2006.

[10] “Universal Frequency-to-Digital Converter (UFDC-1),” Specification and Application Note, 2004

[11] S. Y. Yurish, “Universal smart sensors interface and signal conditioner,” in Proc. IEEE 6th Conference Sensors, Atlanta, USA, Oct 2007, pp. 24–27.

[12] “Novel modified method of the dependent count for high precision and fast measurements of frequency-time parameters of electric signals,” in Proc. IEEE International Instrumentation and Measurement Technology Conference, May 2008, pp. 876–881.

[13] A. Aloisio, P. Branchini, R. Cicalese, R. Giordano, V. Izzo, and S. Loffredo, “Fpga implementation of a high-resolution time-to-digital converter,” in Proc. Nuclear Science Symposium Conference, Oct 2007.

[14] R. Cicalese, A. Aloisio, P. Branchini, R. G. V. Izzo, and S. Loffredo, “Implementation of high-resolution time-todigital converters on two different FPGA devices,” in Proc. WSPC, Oct 2007.

[15] N. Ramalingam, V. K. Varadan, and V. V. Varadan, “Innovative frequency measurement technique used in the design of a single channel frequency to digital converter ASIC,” Smart Materials and Structures, vol. 8, no. 2, pp. 243–251, Apr 1999.

[16] N. V. Kirianaki, S. Y.Yurish, and N. O. Shpak, “Methods of dependent count for frequency measurements,” Measurement, vol. 29, no. 1, pp. 31–50, Jan 2001.

[17] I. B. Vasconcelos and E. J. P. Santos, “A VHDL implementation of a pulse-width and frequency to digital converter,” in Proc. IEEE 14th International Workshop Iberchip, Puebla, 2008.

[18] Edvalj.p.santos,Leonardo,B.m.silva,”Fgpa based sensor implementation with precise Frequency to Digital converter for flow measurement. 978-1-4244-6311-4/10 ©2010 IEEE

[19] http://www.xilinx.com.

[20] http://www.fpgamac.com.